the components or elements is dealt with below, the shape or positional relationship substantially includes an approximate or similar shape or relationship, except for cases where any particular remark is provided and where it is obviously understood that any approximate or similar shape or relationship is not included. The same applies to numerical values and ranges described above.

(Embodiment 1)

A method of manufacturing a CMOSFET (Complementary Metal Oxide Semiconductor Field Effect Transistor) in this embodiment will be described with reference to FIGS. 1 to 16.

Firstly, as shown in FIG.1, a wafer 1 made of mono-crystalline silicon having resistivity of about 10 Ω is subjected to a heat treatment thereby forming a silicon oxide film 2 having a thickness of about 10 nm on its main surface. Thereafter, a silicon nitride film 3 having a film thickness of about 100nm is deposited on this silicon oxide film 2 by a CVD method.

Next, as shown in FIG.2, a photoresist film 4 is formed partially on the silicon nitride film 3 so as to define an element separation region. The silicon nitride film 3 in the element separation region is dry-etched with the photoresist film 4 used as a mask.

Next, the photoresist film 4 is removed. Thereafter, as shown in FIG.3, by using the silicon nitride film 3 as